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Attorney Docket No. 000939-073600US

"Express Mail" Label No. EK026672074US

Date of Deposit: November 2, 1999

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Box Reissue Patent Application
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U. S. Patent and Trademark Office
Washington, D.C. 20231

By: Sara B. McPeak
Sara B. McPeak

ASSISTANT COMMISSIONER FOR PATENTS
REISSUE PATENT APPLICATION
U. S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is the

[X] Patent application for Reissue of U. S. Utility Patent No. 5,683,938, Issued on Nov. 4, 1997
[ ] continuation patent application of
[ ] divisional patent application of
[ ] continuation-in-part patent application of

Inventor(s)/Applicant Identifier: Sang Young Kim, 139-26 An Am-Dong Sung buk-Gu, Seoul Korea; Yung Wook Song, 306-504, Hyundai APT., Gwang Jang Dong, Sung Dong Gu, Seoul, Korea; and Hun Do Kim, 21-34 Gu wi-Dong, Sung Dong –Gu, Seoul, Korea.

For: METHOD FOR FILLING CONTACT HOLES WITH METAL BY TWO-STEP DEPOSITION

[X] This application claims priority from each of the following Application Nos./filing dates:
Korean Patent Application No. 91-18500, filed October 21, 1991 and U. S. Patent Application No. 07/964,362, filed October 21, 1992 and now abandoned.
the disclosure(s) of which is (are) incorporated by reference.

[ ] Please amend this application by adding the following before the first sentence: "This application is a [ ] continuation [ ] continuation-in-part of and claims the benefit of U.S. Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference."

Enclosed are:

[X] A copy of the original printed Patent No. 5,683,938, issued Nov. 4, 1997, is attached.

Reissue Patent Application consisting of:

[X] 1 page cover sheet
[X] 2 page(s) intro/abstract
[X] 3 sheet(s) of [X] formal [ ] informal drawing(s).
[X] 6 page(s) original specification and claims as issued
[X] 22 pages of new claims
[X] A [X] signed [ ] unsigned Declaration & Power of Attorney
[ ] A [ ] signed [ ] unsigned Declaration.
[ ] A Power of Attorney by Assignee with Certificate Under 37 CFR Section 3.73(b).
[ ] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [ ] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.
[ ] A certified copy of a _____ application.
[ ] Information Disclosure Statement under 37 CFR 1.97.
[ ] A petition to extend time to respond in the parent application.
[ ] Notification of change of [ ] power of attorney [ ] correspondence address filed in prior application.
[X] Executed Assent of Assignee and Offer to Surrender Patent

	(Col. 1)		(Col. 2)
FOR:	NO. FILED		NO. EXTRA
BASIC FEE			
TOTAL CLAIMS	88	- 20 =	*68
INDEP. CLAIMS	20	- 2 =	*18
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED			

* If the difference in Col. 1 is less than 0, enter "0" in Col. 2.

SMALL ENTITY			OTHER THAN SMALL ENTITY	
RATE	FEE	OR	RATE	FEE
	$380.00	OR		$760.00
x $9.00 =		OR	x $18.00 =	$1,224.00
x $39.00 =		OR	x $78.00 =	$1,404.00
+ $130.00 =		OR	+ $260.00 =	
TOTAL		OR	TOTAL	$3,388.00

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- [X] Any additional fees associated with this paper or during the pendency of this application.
- [ ] The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b)

[ ] A check for $____________ is enclosed.

2 extra copies of this sheet are enclosed.

Respectfully submitted,
TOWNSEND and TOWNSEND and CREW LLP

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	(Col. 1)	(Col. 2)	SMALL ENTITY			OTHER THAN SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
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INDEP. CLAIMS	20 - 2	= *18	x $39.00 =		OR	x $78.00 =	$1,404.00
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED			+ $130.00 =		OR	+ $260.00 =	
			TOTAL		OR	TOTAL	$3,388.00

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[ ] A check for $_____ is enclosed.

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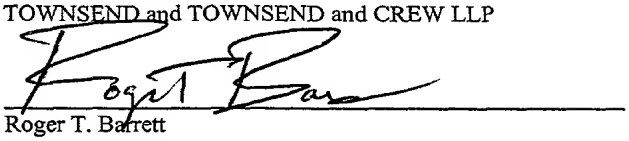

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On November 2, 1999
TOWNSEND and TOWNSEND and CREW LLP
By: Sara B. McPeak
Sara B. McPeak

PATENT
Attorney Docket No.:000939-008700US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Re-Issue Application of:

Sang Young Kim, et al.

U. S. Patent No. 5,683,938

Filed: November 2, 1999

For: METHOD FOR FILLING CONTACT HOLES WITH METAL BY TWO-STEP DEPOSITION

ASSENT OF ASSIGNEE AND OFFER TO SURRENDER PATENT

Assistant Commissioner for Patents
U. S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Hyundai Electronics Industries, Co., Ltd., assignee of U. S. Patent No. 5,683,938 (recorded at Reel 6292, Frame 0064), assents to the above-identified application for reissue of said patent.

Hyundai Electronics Industries, Co., Ltd., hereby offers to surrender U. S. Patent No. 5,683,938.

Hyundai Electronics Industries, Co., Ltd.

Date: October 29, 1999 By: D.S. Chang
Name: D. S. Chang
Title: Director

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Attorney Docket No.: 000939-073600US

PATENT APPLICATION FOR REISSUE OF U. S. UTILITY PATENT NO. 5,683,938 ISSUED ON NOVEMBER 4, 1997

Title: **METHOD FOR FILLING CONTACT HOLES WITH METAL BY TWO-STEP DEPOSITION**

Inventor(s):

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Seoul, Korea

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21-34 Gu wi-Dong, Sung Dong-Gu
Seoul, Korea

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Sara B. McPeak

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Two Embarcadero Center, 8th Floor
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United States Patent [19]

Kim et al.

[54] **METHOD FOR FILLING CONTACT HOLES WITH METAL BY TWO-STEP DEPOSITION**

[75] Inventors: **Sang Young Kim**; **Yung Wook Song**; **Hun Do Kim**, all of Seoul, Rep. of Korea

[73] Assignee: **Hyundai Electronics Industries Co., Ltd.**, Kyoung Ki-Do, Rep. of Korea

[21] Appl. No.: **327,887**

[22] Filed: **Oct. 24, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 964,362, Oct. 21, 1992, abandoned.

[30] **Foreign Application Priority Data**

Oct. 21, 1991 [KR] Rep. of Korea 91-18500

[51] **Int. Cl.**[6] **H01L 21/28**

[52] **U.S. Cl.** 437/192; 437/195; 437/981

[58] **Field of Search** 437/192, 195, 437/189, 190, 981

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US005683938A

[11] Patent Number: 5,683,938

[45] Date of Patent: Nov. 4, 1997

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Primary Examiner—John Niebling
Assistant Examiner—Thomas G. Bilodeau
Attorney, Agent, or Firm—Merchant, Gould, Smith, Edell, Welter & Schmidt, P.A.

[57] **ABSTRACT**

Method for filling contact holes with metals by two-step deposition of selective tungsten layer is disclosed. The selective tungsten thin films are deposited in two steps, thus maximizing the contact filling with tungsten, gaining a stability of metal wires with better step coverage, and enhancing the reliability on semiconductor element.

5 Claims, 3 Drawing Sheets

METHOD FOR FILLING CONTACT HOLES WITH METAL BY TWO-STEP DEPOSITION

This is a continuation of U.S. application Ser. No. 07/964,362 filed Oct. 21, 1992, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a method for filling contact holes with metal in the process steps to fabricate highly-integrated semiconductor device, and more particularly, to a method for filling the contact holes with two-step deposition of the selective tungsten thin films to minimize their surface topography, thus achieving better step coverage of the metal layer.

2. Description of the Prior Art

Generally, as the contact size in semiconductor device is reduced, the aspect ratio of the contact hole becomes larger and as a result, metal with poor step coverage causes the reliability problem to the semiconductor device. To resolve this matter, chemical vapor deposition (CVD) method is attractive for filling the inside of contact holes with selective tungsten thin films, thus better improving the step coverage of metal layer. The CVD process, however, has a troublesome problem associated with the difference of surface topography in contact holes. In the case of filling the contact holes with the highest surface topography with the selective tungsten thin films, the films become overgrown at the contact holes with rather lower surface topography and circuit failure may result between metal wires. To avoid such disadvantage, it is inevitable for the holes with the lowest surface topography to be filled in the first place. Consequently, the aspect ratio of contact holes with the highest step coverage cannot be significantly improved and this unfavorable situation is expected to continue thereafter, as the semiconductor elements become highly integrated and smaller.

It is a principle object of the present invention, therefore, to provide a contact-filling method, in which the selective tungsten thin films are deposited in two steps, thus maximizing the contact filling with tungsten, gaining a stability of metal wires with better step coverage, and enhancing the reliability on semiconductor elements.

The above-said objective should be construed as only one of many possible through the utilization of a few of the more practical and important features and applications of the invention. Many other beneficial results can be obtained by applying the disclosed invention in a different manner or modifying the invention within the scope of the disclosure. Accordingly, other objectives and a fuller understanding of the invention may be had by referring to both the summary of the invention and the detailed description, below, which describe the preferred embodiments and describe the scope of the invention defined by the claims, whose summary and description should be considered in conjunction with the accompanying drawings.

SUMMARY OF THE INVENTION

In order to prevent the metal layers from having poor step coverage due to the difference of surface topography in contact holes, the present invention is characterized by the fabrication steps as set forth hereunder:

As a first step, a field layer, a junction layer, and a gate electrode are formed on the upper part of silicon substrate, respectively. After depositing the first insulating layer over

the upper part of the whole structure, the areas predetermined for the establishment of contact holes on the first-stage insulating layer are removed to form the first contact hole while both the junction layer on the lower part and the gate electrode are exposed;

The second step is to completely fill the contact holes with metal layers and the patterns of conductive layer is formed on the part of the first insulating layer isolated from said metal layers;

The third step is to form the second insulating layer on the upper part of the whole structure, whereby the areas prearranged for the establishment of contact holes on the second insulating layer are removed to form the second contact hole while both the metal layer on the lower part of the first contact hole and the patterns of conductive layer are exposed;

The last step is to fill the second contact hole with metal layers which is connected to the lower part of metal layer and the patterns of conductive layer.

The more practical and important features of the present invention have been outlined above in order that the detailed description of the invention which follows will be better understood and that the present contribution to the art can be fully appreciated. Additional features of the invention described hereinafter also form the subject matter of the claims of the invention. Those skilled in the art can appreciate that the conceptions and the specific embodiments disclosed herein may be readily utilized as bases for modifying or designing other structures for carrying out the same purposes as those of the present invention. Further, those skilled in the art can realize that such modified or newly-designed other structures do not depart from the spirit and scope of the invention as set forth in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and object of the invention, reference should be made to the following Detailed Description of the Invention in conjunction with the accompanying drawings, a brief description of which drawings follow:

FIG. 1A and FIG. 1B are cross-sectional views illustrating that the contact holes in larger depth are unfilled due to the difference of their surface topography when they are formed in accordance with the prior art, and the selective tungsten thin films are deposited into the contact holes in a predetermined thickness;

FIG. 2A through FIG. 2D are cross-sectional views illustrating that contact holes are formed in two step in accordance with the process steps of the present invention and two-step deposition is made available by the selective tungsten thin layers.

The respective reference numerals noted in the detailed description of the invention below refer to the respective reference numerals relating to the pertinent drawing pairs and found as applicable throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1A is a cross-sectional view for fabricating the device with the following process steps. A field oxide layer 3 is deposited on the surface of silicon substrate 1 to give isolation region among the elements, and a N+ or P+ junction layer 2 is formed on the silicon substrate. Next, after growing a gate oxide layer 4, a polysilicon is formed

as a gate electrode 5. The first insulating oxide layer 6 is deposited on the upper part of the whole structure, and a polysilicon 7 for wiring is formed on the areas predetermined for the establishment of contact holes. Next, after depositing the second insulating oxide layer(8) on the upper part of the whole structure, the pattern process using a photoresist film is employed to form the contact holes at the predetermined areas between the first insulating layer 6 and the second insulating layer 8.

FIG. 1B is a cross-sectional view, as shown in FIG. 1A, to illustrate that deeper contact holes 20 are unfilled due to the difference of their surface topography, when the contact holes 20 are formed in accordance with the prior art and the selective tungsten thin films are deposited to the shallowest holes.

FIG. 2A through FIG. 2D are cross-sectional views illustrating that the contact holes are formed in two steps in accordance with the process steps of the present invention and the two-step deposit is made available by the selective tungsten thin layers.

FIG. 2A is a cross-sectional view for fabricating the device with the following process steps. After growing a field oxide layer 3 and a gate oxide layer 4 on the silicon substrate 1, a N+ or P+ junction layer 2 is formed. A gate electrode 5 is formed on the upper part of a gate oxide layer 4, and the first insulating oxide layer 6 is deposited on the whole structure. The prior art covers the above process steps. In the next process, a photoresist film is used to form the contact pattern mask, the first insulating oxide layer 6 exposed hereto is etched by wet and/or dry etching, and the first contact hole 30 is formed while the gate electrode 5 and N+ or P+ junction 2 are exposed.

FIG. 2B is a cross-sectional view illustrating that the first contact hole 30, as fabricated in FIG. 2A, is filled with the selective tungsten thin films 9 by the CVD method. The selective tungsten thin films 9 fill the first contact hole 30, the selective films are overgrown appropriately to prevent misalignment with a second contact hole to be formed above the first contact hole.

FIG. 2C is a cross-sectional view illustrating that a polysilicon 7 for wiring is placed on the areas predetermined for the establishment of contact holes on the upper part of the first insulating layer 6. After depositing the second insulating oxide layer 8 on the upper part of the whole structure, the etching by the contact pattern mask is made to the second insulating layer 8 placed on the first contact hole 30 and the polysilicon 7 for wiring to form a second contact hole 40 over each of the first contact hole and the polysilicon 7.

FIG. 2D is a cross-sectional view illustrating that the second contact hole 40 above the first contact hole 30, as fabricated in FIG. 2C, is almost filled by the CVD method with selective tungsten thin films 10 in contact with the selective tungsten thin films 9 of the first contact hole 30, and that the second contact hole 40 above the polysilicon 7 is simultaneously almost filled with selective tungsten thin films 10 by the CVD method.

As described above, the object of the present invention is to provide a method for filling the contact holes which have a rough surface topography with metal layers, in which, the first insulating oxide layer is provided. The tungsten thin

films are deposited in the first contact hole and on the upper part. the second insulating oxide layer is formed. Next, the second contact hole is formed on the upper part of the first contact hole and on the areas predetermined for the establishment of the contact holes. Then, the second contact hole becomes almost filled with the selective tungsten thin films. thus achieving better step coverage of metal wire at the contact holes.

Although this invention has been described in its preferred forms with a certain degree of particularity. it will be appreciated by those skilled in the art that the present disclosure of the preferred forms has been effected only by way of example, and that numerous changes in the details of the construction. combination and arrangement of parts may be resorted to without departing from the spirit and scope of the invention.

What is claimed is:

1. A method for filling contact holes with metal by two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into the first plurality of contact holes, entirely. the first metal layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern. the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

2. A method according to claim 1, wherein the first metal layer and subsequently the second metal layer are formed by chemical vapor deposition method.

3. A method according to claim 1, wherein the second metal layer filled in each of the second plurality of contacts holes has substantially equal depth.

4. A method according to claim 1, wherein the first and second metal layers are selective tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second metal layers of the selected tungsten layers, respectively.

5. A method for filling contact holes with metal by a two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

* * * * *

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into entire first plurality of contact holes by one single step, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes;

6. A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into the first plurality of contact holes, entirely, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

7. A method according to claim 1, wherein the first conductive material layer and subsequently the second conductive

material layer are formed by a chemical vapor deposition process.

8. A method according to claim 1, wherein the second conductive material layer filled in each of the second plurality of contacts holes has substantially equal depth.

9. A method according to claim 1, wherein the first and second conductive material layers comprise first and second tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second tungsten layers, respectively.

10. A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into entire first plurality of contact holes in a continuous step, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

11. A method according to claim 10, wherein said steps of forming said first and said second conductive material layers comprise filling said first and said second plurality of contact holes, respectively.

12. A method of forming a substrate with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming a first contact hole by removing a portion of the first insulating layer to expose said junction layer, the first contact hole having a tapered upper portion;

forming a first conductive material layer into the first contact hole, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first contact hole;

forming a second contact hole by removing portions of said second insulating layer to expose the first conductive

material layer; and

forming a second conductive material layer into said second contact hole to contact the first conductive material layer.

13. A method as in claim 12, further comprising:

forming a third contact hole by removing portions of the second insulating layer to expose the conductive layer pattern; and

forming the second conductive material layer into the third contact hole to contact the conductive layer pattern.

14. A method as in claim 12, wherein said first and said second conductive material layers comprise a metal.

15. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first plurality of contact holes having a tapered upper portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and

the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

16. A method as in claim 15, wherein said first and second conductive material layers comprise first and second metal layers.

17. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion;

forming a first conductive material layer into the first contact hole, filling said first contact hole entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer

to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

18. A method as in claim 17, wherein said first conductive layer pattern comprises a gate electrode.

19. A method as in claim 17, wherein said first and second conductive material layers comprise first and second metal layers.

20. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions

of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

21. A method as in claim 20, wherein said first and second conductive material layers comprise first and second metal layers.

22. A method as in claim 20, wherein said first conductive layer pattern comprises a gate electrode.

23. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and said first and said second regions;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and second regions, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into, and filling entirely, the first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material

layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

24. A method as in claim 23, wherein said first region comprises a junction layer.

25. A method as in claim 23, wherein said second region comprises a gate electrode.

26. A method as in claim 23, wherein said first and second conductive material layers comprise first and second metal layers.

27. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively;

forming a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

28. A method as in claim 27, wherein said first and second conductive material layers comprise first and second metal layers.

29. A method as in claim 27, wherein said first plurality of contact holes have a tapered upper portion.

30. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer, the first

plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

31. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and

the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

32. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion;

forming a first metal layer into the first plurality of contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second and third contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

33. A method as in claim 32, wherein said first conductive layer pattern comprises a gate electrode.

34. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer and first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

35. A method as in claim 34, wherein said first

conductive layer pattern comprises a gate electrode.

36. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the first region and the second region;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and said second region, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

37. A method as in claim 36, wherein said first region comprises a junction layer.

38. A method as in claim 36, wherein said second region comprises a gate electrode.

39. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

40. A method as in claim 39, wherein said first plurality of contact holes have a tapered upper portion.

41. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern;

forming a first contact hole by removing portions of the first insulating layer to expose said first conductive layer pattern;

forming a first conductive material layer into the first contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and said third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

42. The method of claim 41, wherein said first conductive material layer comprises a metal.

43. The method of claim 42, wherein said metal comprises tungsten.

44. The method of claim 41, wherein said first

conductive material layer comprises polysilicon.

45. The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode.

46. The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

47. The method of claim 41, further comprising a junction layer on said substrate.

48. The method of claim 47, wherein said junction layer comprises a N+ junction layer.

49. The method of claim 47, wherein said junction layer comprises a P+ junction layer.

50. The method of claim 41, wherein said first conductive layer pattern comprises polysilicon.

51. The method of claim 41, wherein said first insulating layer comprises a first oxide layer.

52. The method of claim 41, wherein said step of forming said first contact hole comprises a photoresist process.

53. The method of claim 41, wherein said step of forming said first contact hole comprises a wet etch process.

54. The method of claim 41, wherein said step of forming said first contact hole comprises a dry etch process.

55. The method of claim 47, wherein said step of

forming said first contact hole further exposes said junction layer.

56. The method of claim 41, wherein said first contact hole has a tapered upper portion.

57. The method of claim 41, wherein said step of forming said first conductive material layer comprises a CVD process.

58. The method of claim 41, wherein said second conductive layer pattern comprises polysilicon.

59. The method of claim 41, wherein said second insulating layer comprises a second oxide layer.

60. The method of claim 41, wherein said step of forming said second and said third contact holes comprises a photoresist process.

61. The method of claim 41, wherein said step of forming said second and said third contact holes comprises a wet etch process.

62. The method of claim 41, wherein said step of forming said second and said third contact holes comprises a dry etch process.

63. The method of claim 41, wherein said step of forming said second conductive material layer comprises a CVD process.

64. A semiconductor device comprising:
a semiconductor substrate having an oxide layer, a

junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion;

a first metal layer filling said first plurality of contact holes so that said first metal layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first metal layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first metal layer and said conductive layer pattern; and

a second metal layer filling said second plurality of contact holes, said second metal layer in contact with said first metal layer and said conductive layer pattern.

65. A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said junction layer and said gate

electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said conductive layer pattern.

66. A semiconductor device comprising:

a semiconductor substrate having an oxide layer and a first conductive layer pattern;

a first insulating layer overlying portions of said oxide layer and said first conductive layer pattern, said first insulating layer having a first plurality of contact holes of substantially equal depth over said first conductive layer pattern;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said first conductive layer pattern;

a second conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said second conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said second conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said second conductive layer pattern.

67. The device of claim 66, wherein said conductive material layers comprise a metal.

68. The device of claim 67, wherein said metal comprises tungsten.

69. The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode.

70. The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

71. The device of claim 66, wherein said first conductive material layer comprises polysilicon.

72. The device of claim 66, further comprising a junction layer on said substrate.

73. The device of claim 72, wherein said junction layer comprises a N+ junction layer.

74. The device of claim 72, wherein said junction layer comprises a P+ junction layer.

75. The device of claim 66, wherein said first conductive layer pattern comprises polysilicon.

76. The device of claim 66, wherein said first

insulating layer comprises a first oxide layer.

77. The device of claim 66, wherein said first plurality of contact holes are formed by a photoresist process.

78. The device of claim 66, wherein said first plurality of contact holes are formed by a wet etch process.

79. The device of claim 66, wherein said first plurality of contact holes are formed by a dry etch process.

80. The device of claim 72, wherein said first plurality of contact holes expose said junction layer.

81. The device of claim 66, wherein said first plurality of contact holes have tapered upper portions.

82. The device of claim 66, wherein said first plurality of contact holes are formed by a CVD process.

83. The device of claim 66, wherein said second conductive layer pattern comprises polysilicon.

84. The device of claim 66, wherein said second insulating layer comprises a second oxide layer.

85. The device of claim 66, wherein said second plurality of contact holes are formed by a photoresist process.

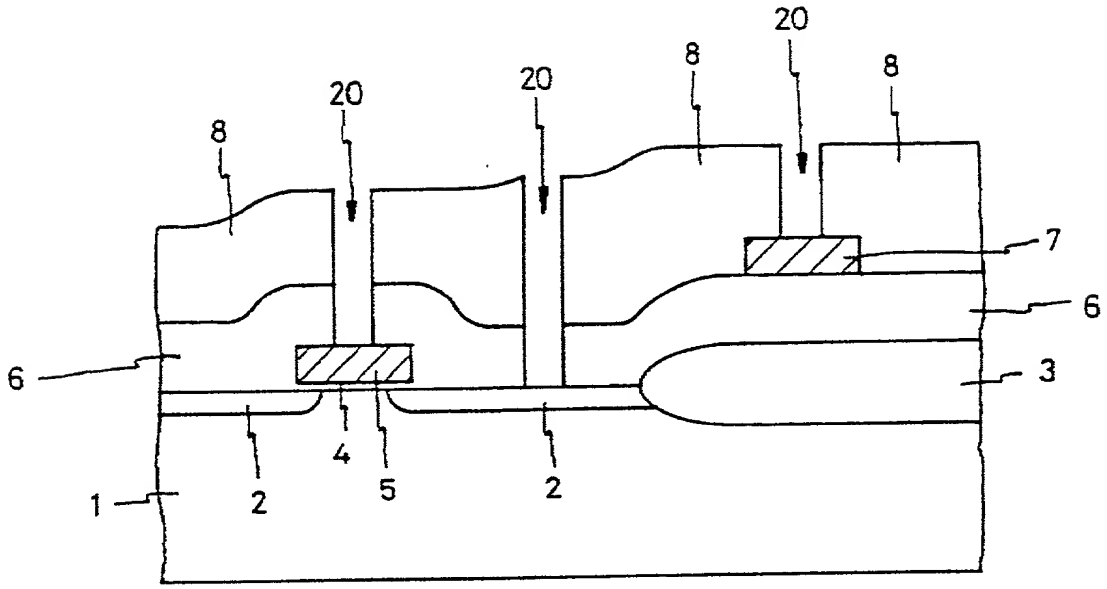
86. The device of claim 66, wherein said second plurality of contact holes are formed by a wet etch process.

87. The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. The device of claim 66, wherein said second plurality of contact holes are formed by a CVD process.

"PRIOR ART"

Fig. 1A



"PRIOR ART"

Fig. 1B

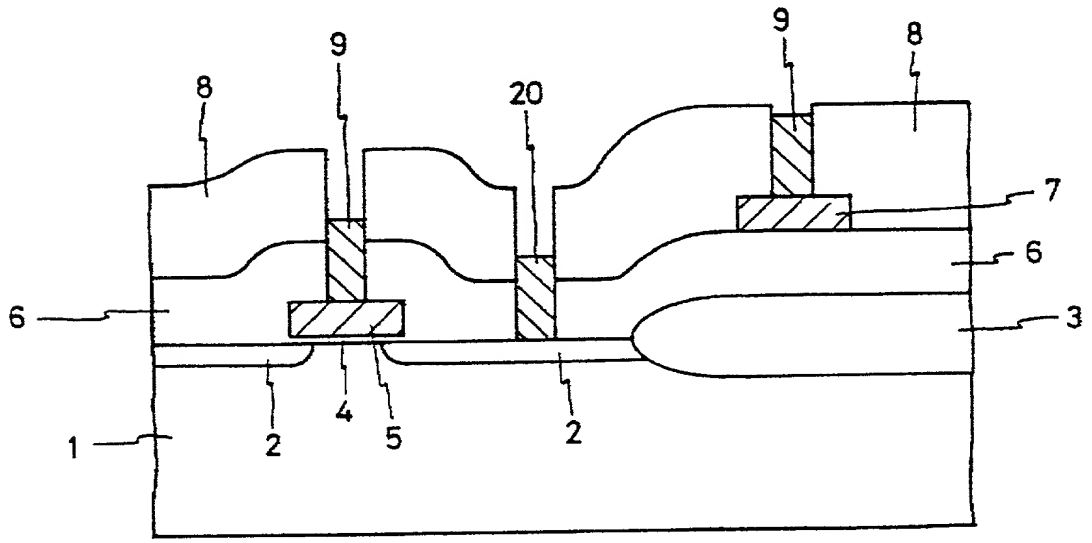


Fig. 2A

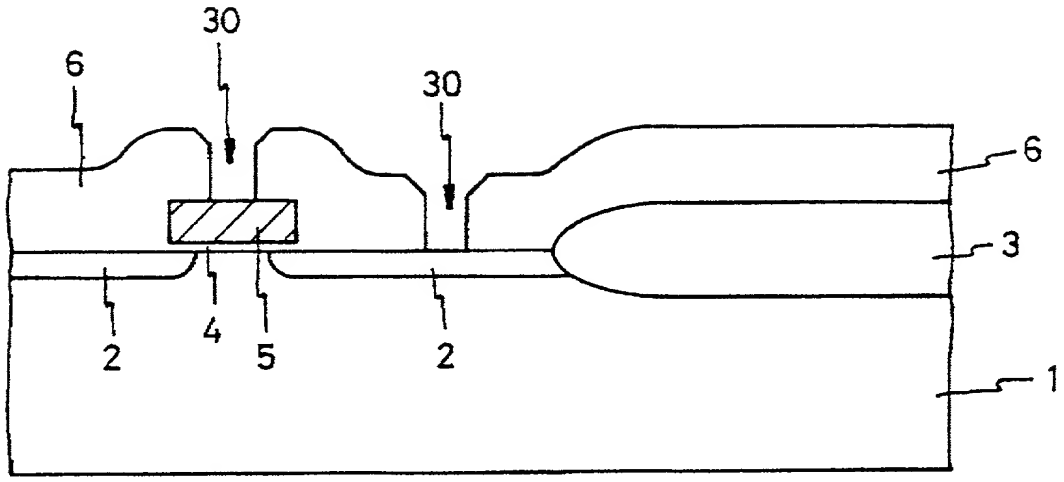


Fig. 2B

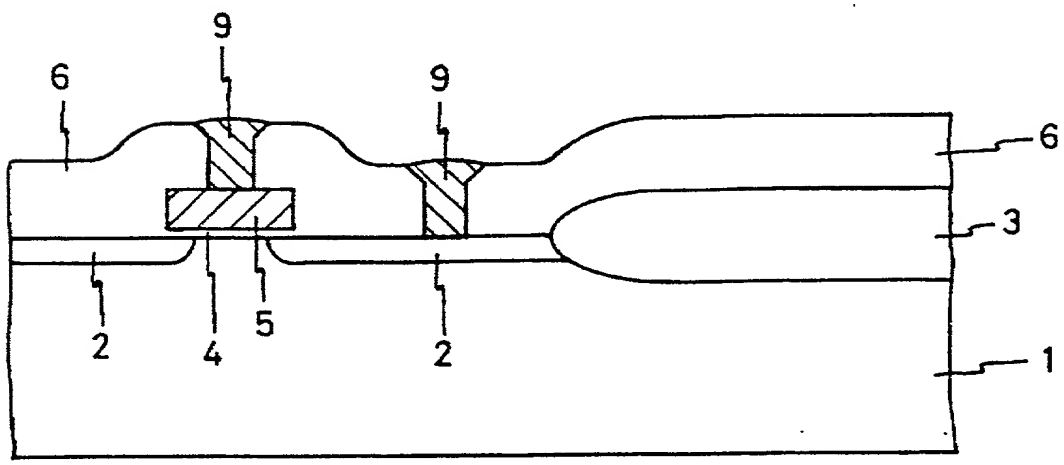


FIG. 2C

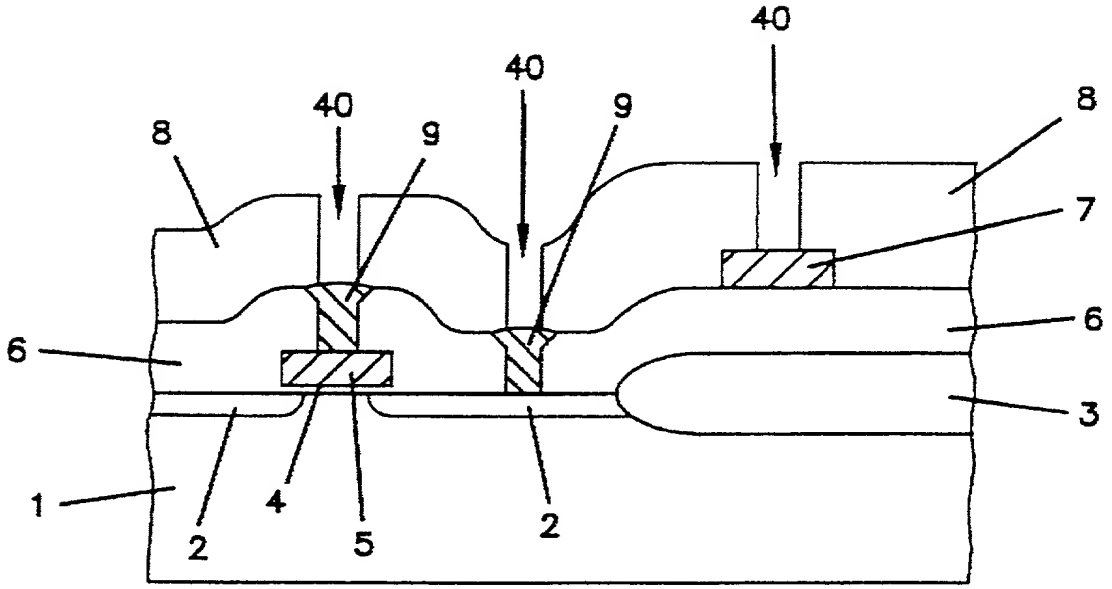
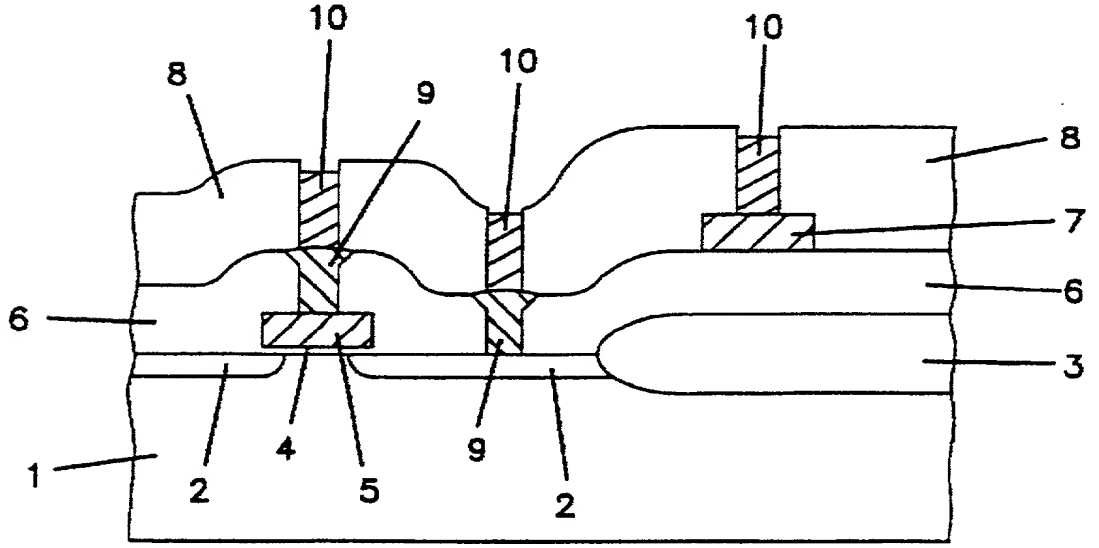


FIG. 2D



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a reissue patent is sought on U. S. Patent No. 5,683,938 entitled METHOD FOR FILLING CONTACT HOLES WITH METAL BY TWO-STEP DEPOSITION, the specification of which is attached hereto.

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I verily believe the original patent 5,683,938 is partially inoperative or invalid by reason of the patentee claiming less than he had a right to claim in the patent. One error of the original patent corrected by the present reissue application is that the independent claims of the original patent require the deposition of metal layers, whereas those skilled in the art at the time of the invention would realize that the present invention equally applies to the deposition of other conductive layers, such as polysilicon. The failure to include claims depositing conductive layers is an error that the present reissue application corrects.

All errors corrected by the present reissue application arose without deceptive intent on my part as applicant.

I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign applications(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
Korean	91-18500	October 21, 1991	Yes

I claim the benefit under Title 35, United States Code, Section 120 of any United States or international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or international application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status
07/964,362	10/21/92	Abandoned

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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SANG YOUNG KIM	YUNG WOOK SONG	HUN DO KIM
Date 10.29.1999.	Date 10.29.1999	Date 10.29.1999

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